PROCESSING AND RELIABILITY ISSUES FOR EUTECTIC AUSN SOLDER JOINTS

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Eutectic AuSn solder is increasingly used in high reliability and/or high temperature applications where conventional SnPb and Pb-free solders exhibit insufficient strength, creep resistance, and other issues. These applications include hybrid microelectronics (particularly flip chips), microelectromechanical systems (MEMS), optical switches, LEDs, laser diodes, radiofrequency (RF) devices, and hermetic packaging for commercial, industrial, military, and telecommunications applications. For most of these applications, AuSn provides the additional benefit of not requiring flux during reflow, significantly reducing the potential for contamination and pad corrosion.

However, the materials and processing considerations are substantially different than for conventional solders. Many companies struggle with issues such as poor solder flow, excessive void formation, variable reflow temperature (arising from off-eutectic compositions), heterogeneous phase distribution, and others, all contributing to development delays, process yield loss, and field reliability issues. This paper reviews the critical issues in material and process selection, as well as long-term diffusion and mechanical stability.

Eutectic AuSn is widely used in high temperature and high reliability applications due to excellent mechanical and thermal properties (particularly strength and creep resistance) and its ability to be reflowed without flux. Other Pb-free and traditional Pb-based eutectic solders suffer by comparison due to a variety of problems:

- The required fluxes are responsible for bond pad corrosion, as well as residues that compromise MEMS, optics, and hermetic packages (fluxes are generally forbidden for hermetic telecom applications)
- Excessive creep or stress relaxation, leading to progressive alignment degradation in many optical applications
- Low strength (eutectic AuSn is erroneously associated with embrittlement of conventional SnPb and Pb-free solders on Cu lines, when in fact the culprits are irregularly formed Au-Ni-Sn intermetallics[35])
- Low thermal conductivity (though this problem is overstated, as thermal conductivity must be considered in conjunction with the solder joint thickness)

The applications covered in this paper include: flip chips for microelectronics[4,8,9,27,33] and optoelectronics[4,27] such as MEMS optical switches[12,13], photonic circuits[14], and fiber attachment[23]; LEDs[5,24,25]; GaAs and InP laser diodes[3,6,10,11,22,37]; hermetic packaging[17,21]; and RF devices[26].

While components with AuSn solder joints have demonstrated reliable performance in demanding environments for over 30 years, the performance is based on reflow processes that produce repeatable, void and defect-free joints. This paper was motivated by numerous requests from startups and established companies for advice on solder joint design, acceptable material combinations, and reflow process development.

/ PHASE DIAGRAM

Many of the key issues associated with AuSn soldering can be ascertained from the binary phase diagram, shown in Figure 1. The most notable features are steep liquidus lines, particularly on the Au-rich side of the eutectic composition (71 at% Au/29 at% Sn, or 80 at% Au/20 at% Sn by weight), and the numerous intermetallic “line” compounds at ambient temperature.

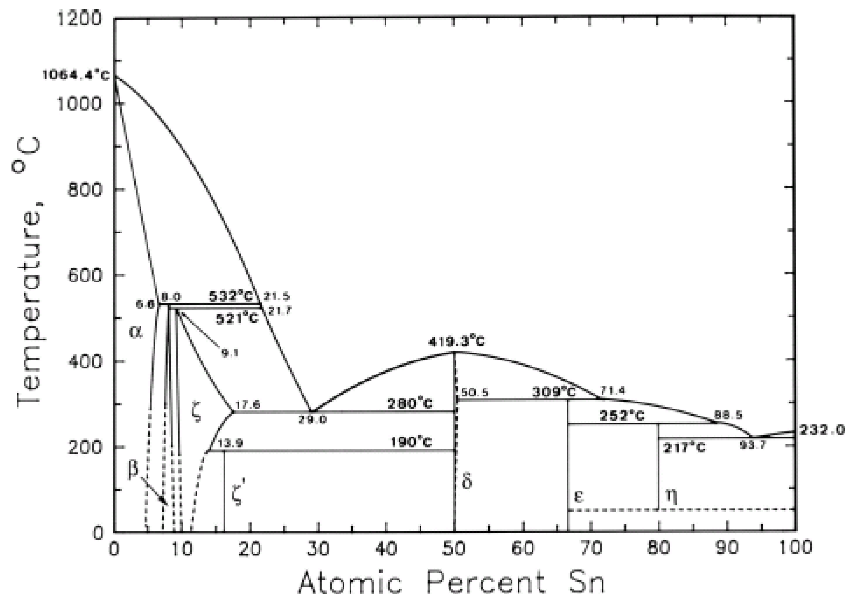

Figure 1: Au-Sn binary phase diagram (adapted from [1]).

When using eutectic solder (preforms, pastes, or platings) and metallizations terminated with Au layers, the resulting solder joint will have a melting point much higher than 280 °C due to diffusion/leaching of the Au metallization into the solder. This can be advantageous for two reasons: secondary reflow of other components can be performed at the same temperature without disturbing the initial solder joint, and the higher remelt temperature generally implies greater creep resistance. However, the component may be difficult or impossible to rework; even if the two bonded adherends can be separated (by shearing or “hot-lifting”), irregular/uneven intermetallics will be left on both surfaces and prevent subsequent reflow. Additionally, solidification (“freezing”) may occur during reflow, leading to poor wetting and associated insufficient bond coverage and strength.

These disadvantages can be addressed by biasing the composition of the solder to the Sn-rich side, so that the eutectic composition is obtained after complete dissolution of the Au metallization. For preforms and pastes, this approach may be problematic due to variability in solder composition, which is one of the reasons why many applications employ AuSn deposited by evaporation, sputtering, or electroplating.

At the eutectic composition, the following compounds should be observed upon cooling: $L \rightarrow \xi + \delta \rightarrow \xi' + \delta$. Generally, the microstructure is a fine mixture of ξ' and δ in the bulk of the joint, with predominantly ξ' layers at the metallization interfaces. [Typical microstructures are shown in references 4, 20, and 23.]

When Au and Sn layers (single or multiple of each) are employed, sequential formation of η, ε, δ, and ξ' is expected at the Au-Sn interface[30,31]. Generally, this approach is known as transient liquid phase (TLP), rather than eutectic, bonding. The advantage of TLP bonding is that reflow temperatures between the melting points of Sn (232 °C) and the eutectic can be employed. However, longer process times will be required, either at reflow or during subsequent annealing; furthermore, if the reaction is not completed, microstructural (and residual stress) evolution will continue over time. These disadvantages can be reduced by using thinner, multiple layers (the total number of layers will be dictated by the flatness of the two surfaces to be bonded – the total layer thickness should be greater than 3 times the roughness[38]). Thinner layers minimize the diffusion distances for Au and Sn, and hence the time required to obtain the eutectic composition.

The phase diagram also provides guidance regarding mechanical properties. All of the intermetallics on the Sn-rich side of the diagram are "line" compounds, with extremely limited solubility ranges. These compounds generally exhibit high strength and creep resistance, at the expense of limited ductility (brittleness). As will be discussed in a subsequent section, however, the eutectic phases do possess moderate ductility in addition to excellent creep resistance, and are much less brittle than CuSn intermetallics (common in SnPb and Pb-free solders on Cu metallization or substrates)[35,36].

/ METALLIZATION

Selection of appropriate coatings for the two surfaces to be bonded is critical for reliable soldering with AuSn. The general requirements are:

- Contact/adhesion layer
- Barrier diffusion layer
- Cap layer

The contact/adhesion layer is particularly necessary for semiconductors and ceramics, as most metals will not bond directly with these covalent materials; contact layers are not usually required for metal substrates. The barrier diffusion layer must both bond well to the contact layer and be either non-reactive to Sn (intrinsic) or thick enough to prevent complete dissolution/ intermetallic formation during reflow and subsequent aging (extrinsic). The cap layer prevents oxidation of the surface prior to reflow, and is invariably composed of pure Au for compatibility with AuSn solder.

A wide range of material combinations can be used. Typical metal stacks and thicknesses (if available) are presented in Table 1. Generally, TiW/Au or Ti/Pt/Au (contact/barrier/cap layer, respectively) is used on semiconductors and ceramics, while Ni/Au is employed for metals. The Ni can be either electrolytic (pure Ni) or electroless (2-14% P), but the latter is more common due to lower cost. Studies of different barrier layers are provided for Ni, Pt, and Pd[2] and deposited NiSn and AuSn intermetallics on TiW[3].

Table 1: Substrate materials and their typical metallizations & metallization thicknesses.

Substrate	Metallization	Thickness (um)	Ref.
Si	Ti/Cu/Ni Ti/Cu Ti/Pt/Au TiW/Au	0.2/0.8/10 0.5/0.3 - -	4 5 6,7 8,9
GaAs	Ti/Pt/Au Cr/Pt/Au Ti/W(N)/Au	- - -	10,11 7 12,13
InP	Ti/W/W-AuSn Ti/W/W-NiSn Pd/Ge/Sn Pd/Ge/In/Sn	0.1/0.05-0.2/0.2 0.1/0.05-0.2/0.2 - -	3 3 14 14
AlN	Ti/Mo/Pt	0.08/0.1/1	15
BN	Ti/Pt/Au	-	11
Al_2O_3	Ti/Pt Ni/Au Ti/W/Au	0.03/0.25 - -	15 12 16
Kovar	Ni/Au	0.3/1.0 2.5/1.3-7.6	17 18
Cu	Ni/Au	2.5/1.3-7.6 5/0.1 5/1	18 19 20

For barrier layers that react with Sn, the dissolution rate depends on a number of factors:

- Solder joint thickness
- Peak reflow and storage temperatures
- Time at those temperatures
- Grain morphology and residual stresses in the barrier layer

A particular example is provided to illustrate consumption of the barrier layer, based on the work of Song et al.,[19, 40] and shown on Figure 2. The two papers evaluated AuSn bumps with Ni under-barrier metallization (UBM) on Cu[19], as well as Cu alone[40]. The growth of both Au-Ni-Sn and CuSn intermetallics at the solder/metal interface exhibits square-root dependence with time, typical of diffusion-controlled processes, though the rate of consumption of Ni is lower by a factor of ~2.

Non-reactive barrier metals such as W, particularly when coupled with overlayers of NiSn or AuSn intermetallics, can effectively eliminate barrier metal consumption[3].

For nominally similar materials, reflow, and storage conditions, the consumption rates can vary substantially. As barrier metal grain size decreases, consumption rates will be increased due to enhanced grain boundary diffusion (contributing to bulk diffusion). Residual stresses associated with various phases may not only modify diffusion rates, but also be sufficiently high to initiate yield and cracking[32].

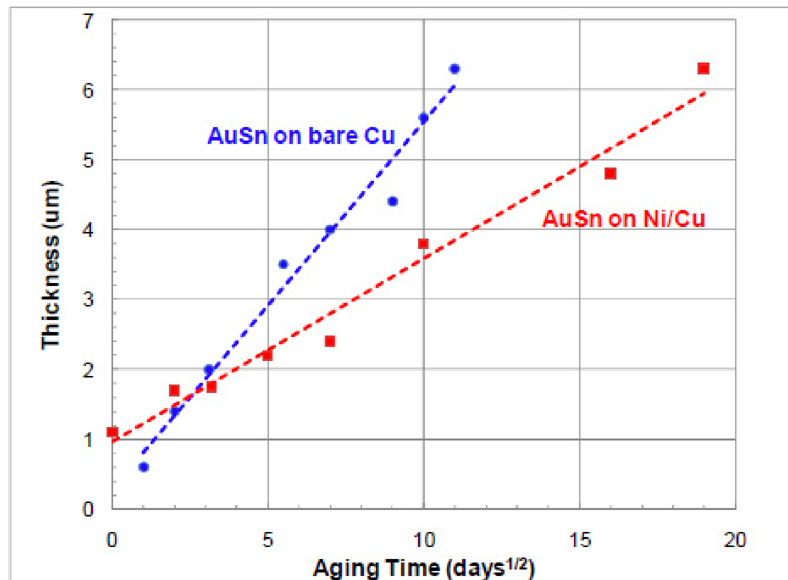

Figure 2: Consumption of barrier metallization by intermetallic versus time at 200°C for eutectic AuSn solder on Ni under bump metallization (UBM) and bare Cu[19,40].

/ SOLDER TYPES & DEPOSITION METHODS

For the studies covered in this paper, the types of solder include preforms, pastes, and deposited films. Film deposition techniques include sputtering, evaporation, and electroplating, involving either single or multiple layers. Brief overviews of the advantages and limitations of each are as follows, along with the associated work referred to in this paper:

- Preform:
  - Advantages: ease of use; does not rely on solder spreading for joint coverage
  - Limitations: composition consistency; oxidation; placement accuracy; low volume process
  - References: 2,5,10,23,37
- Paste:
  - Advantages: compatible with high volume processes, including photoresist processes for solder placement control
  - Limitations: flux required (MEMS, flip chips, and optoelectronics except LEDs excluded); composition control; voids due to trapped gas;
  - References: 19, 20
- Sputtered film:
  - Advantages: composition control
  - Limitations: trapped Ar and possible voiding; low-to-mid volume process; capital expenditure and process control; limited deposition rate
  - References: 38
- Evaporated film:
  - Advantages: composition control
  - Limitations: Au spitting and associated spherical debris/contamination; low-to-mid volume process; capital expenditure and process control; limited deposition rate
  - References [3,11,14,22 for single layer; 7 for multilayer]
- Electroplated film:
  - Advantages: high volume; high deposition rate; composition control; compatibility with existing photoresist processes for solder placement control
  - Limitations: process sensitivity (see [28] for a description of key parameters)
  - References: [6,12,13,15,24,25,28 for single layer; 27,29 for multilayer]

Generally, electroplating of single layers with the eutectic composition or multiple layers of alternating Au^5Sn (ξ') and AuSn (δ) is regarded as having the potential for the most manufacturable, high volume process. However, for proof-of-concept and/or low volume parts, preforms, sputtering, or evaporation may be acceptable.

/ PROCESSING

Guidance on actual process conditions is the most difficult to provide, given differences in: size, weight, flatness, and the coefficient of thermal expansion (CTE) for components & substrates; solder joint size and gas access during reflow; reflow equipment
(ovens, die bonders, IR/laser reflow, hot plates, etc.); associated thermal mass and heating/cooling rates; and more. The following statements are generally true:

- A wide variety of components have been successfully bonded in terms of solder wetting, void content, microstructural uniformity, and subsequent high process yields
- Close CTE matching of the component and substrate is recommended to reduce bonding stresses and associated cracking, though large joints between Cu and Kovar (CTE~10.5 ppm/°C) are possible[18]
- Reducing environments like forming gas (N_2/H_2 mix with greater than 5% H_2) are not necessary, but enable larger process windows and greater process consistency
- For surfaces with some oxide present (preforms; deposited films where there was venting to air between AuSn and Au deposition; overheated Au-coated parts wherein Sn has diffused to the surface), forming gas alone is insufficient, and some mechanical pressure/scrubbing may be required to break up and dissolve the oxide film
- High heating rates (50°C/min or higher) are usually required
- Equally high cooling rates are typical, but substrate and/or component cracking will indicate if the cooling rate and/or CTE mismatch is too high

Particular solder process parameters for a variety of applications and bonding equipment are summarized in Table 2.

Table 2: Typical soldering parameters for eutectic AuSn solder. The studies highlighted in bold are full process matrices. (“?”: unknown; “-“: none; and FG: forming gas [N_2/H_2 mix indicated])

Application (equipment)	Reflow Flux/Gas	Preheat (°C)	Heat. Rate (°C/min)	TAL (sec)	Peak Temp (°C)	Cool. Rate (°C/min)	Ref.
General	95/5FG	-	<50	240-300	320-340	<50	21
General(reflow oven)	?	-	?	65	320	?	4
General (heating plate)	85/15FG	-	75	420	300-350	power off	3
General (reflow oven)	Fluxes, N_2	150	250	25-75	320	250	20
InP laser diode (heating plate)	90/10FG	220	180	10	350	N_2 blow	6
InP laser diode (IR lamp)	H_2	-	5 sec	10-120	320	?	7
Laser diode (die bonder)	Ar	-	900	120	290-310	100	10
GaAs laser diode (die bonder)	80/20FG	-	50-150	5	325-355	400	22
Lensed fiber (soft beam)	?	-	5 sec	25-75	300-345	5 sec	23
LED (die bonder)	?	200	?	20	310	?	24
LED (pick & place)	Fluxes			5-8	305-325		25
RF devices (die bonder)	90/10FG	240	110	310	305	450	26
Flip chip (reflow oven)	?	215	180	10	330	?	8

/ MATERIAL CHARACTERIZATION: MECHANICAL PROPERTIES

The mechanical behavior of solders and intermetallic compounds, especially for use as inputs in finite element analysis (FEA), are typically based on measurements obtained from bulk samples (often produced by arc melting). However, the values obtained from such measurements are usually misleading, due to significant differences in grain size, residual stresses, and mechanical constraint compared to typical solder joints, joint geometries, and material combinations.

Table 3 summarizes the mechanical properties of metals, solders, and relevant intermetallic compounds obtained on actual solder joints or thin film samples. The intermetallic data shown here is entirely from the work of Chromik et al.[35,36], which employed nanoindentation – they provide a detailed discussion of the advantages and limitations of nano-indentation compared to bulk techniques (die and lap shear; resonance; micro-indentation). That same technique was also used to obtain indentation creep data, shown in Figure 3, which validates the high creep resistance of both individual AuSn & $Au^{5}Sn$ phases as well as the eutectic composition itself[35].

Table 3: Summary of mechanical properties of relevant metals, solder alloys, and intermetallic compounds.

Material	E (GPa)	ν	CTE (ppm/C)	σ_Y (MPa)	H (GPa)	Ref.
Au	83	0.42	14.4	207	1.03	34,35
Sn	41	0.33	23.8	56	0.11	34,35
Cu	114	0.34	16.4	52	1.7	34,35
Au80Sn20	74	0.4	16	276	1.3	34,35
Sn63Pb37	32	0.4	25	34		34
Sn96.5-Ag3.5	53	0.4	22	49	0.16	36
β□(8 at% Sn)	88	0.33*		400	1.2	35
Au_5Sn (ξ')	76	0.4		830	2.5	35
AuSn (δ)	87	0.3		370	1.1	35
$AuSn_2$ (ε)	103	0.33*		970	2.9	35
$AuSn_4$ (η)	39	0.31		400	1.2	35
Ag_3Sn	88	0.33*		970	2.9	36
Cu_6Sn_5	119	0.33*		2200	6.5	36
Cu_3Sn	143	0.33*		2100	6.2	36

/ MATERIAL CHARACTERIZATION: DIFFUSION

The effect of Sn diffusion into and subsequent consumption of barrier metal layers was discussed previously. Here, the interdiffusion of Au and Sn is reviewed to provide guidance for applications using single or multiple layers composed of Au and Sn, such as TLP bonding. Somewhat surprisingly, while Sn is the lower melting temperature element, Au is the faster diffusing species when bulk (interstitial) diffusion dominates, due to its lower atomic radii[30,31,32,39]. As the grain size of the Au layer(s) decreases, interdiffusion may be equal or the situation reversed due to faster diffusion of Sn along Au grain boundaries[32]. Differences in interdiffusion rates drive the initiation and growth of Kirkendall voids; an example can be seen in Reference 30 (Figure 2 of that paper).

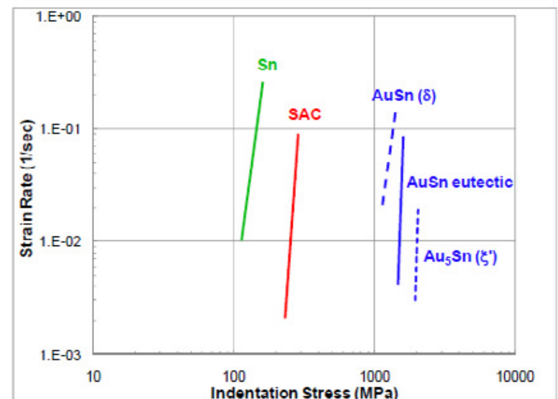

Figure 3: Creep strain rate versus indentation stress for solders and intermetallics, as measured by nanoindentation[35].

Excellent measurements and analysis of intermetallic formation rates at varying annealing temperatures were performed by Yamada et al.[31,39]. Diffusion couples were composed of a single layer of Au between two layers of Sn. In all cases, the three intermediate Au-Sn intermetallic compounds (AuSn4, AuSn2, and AuSn) exhibited a power law relationship with annealing time, and the ratios of each layer thickness to the total intermetallic layer thickness remained constant at a given temperature. The ratio decreased with increasing temperature for AuSn4, while increasing for AuSn2 and AuSn[31].

The total intermetallic layer thickness, l, as a function of time, t, was described according to the following equations:

$$l = k \cdot \left(\frac{t}{t_o}\right)^n$$

and

$$k = k_o \cdot \exp\left(-\frac{Q}{RT}\right)$$

where the exponent, n, and proportionality constant, k, depend on temperature, to and ko are constants, Q is the activation energy, R is the gas constant (8.3144 J/mol-K), and T is the temperature in Kelvin.

An assessment of the intermetallic layer thicknesses at a given temperature and time is illustrated in Figure 4a. The cumulative layer thickness as a function of annealing time and temperature is illustrated in Figure 4b. Fits of Equation 1 are shown, with associated time exponents. The constants in Equation 2 were subsequently

The behavior of thinner deposited layers is expected to be different due to the effects of grain boundary diffusion of Sn, but these studies nonetheless provide a framework for evaluation and analysis.

/ LONG TERM RELIABILITY

Given its high strength and creep resistance, solder joints composed of eutectic AuSn are extremely stable in a broad range of harsh environments. These include thermal cycling from -55 to +125°C[5,8,9,13], high temperature storage from 75 to 150°C [5,9,18], high temperature/high humidity in 121°C autoclaves[9], die or double lap shear after extended aging up to 250°C[18,33], and extended operational performance for laser diodes[11,37].

The primary reliability issues arise from defects introduced during processing (voids, irregular phase formation, weak interfaces due to insufficient barrier metals, etc.) that act as crack initiation sites. While the previous section demonstrated that the two eutectic intermetallic phases possess some ductility, bulk solder joint fracture is typically brittle, and hence linear elastic fracture mechanics is the best methodology for estimating lifetime. Worst-case defect sizes should be based on the limits of non-destructive evaluations & process monitoring capability.

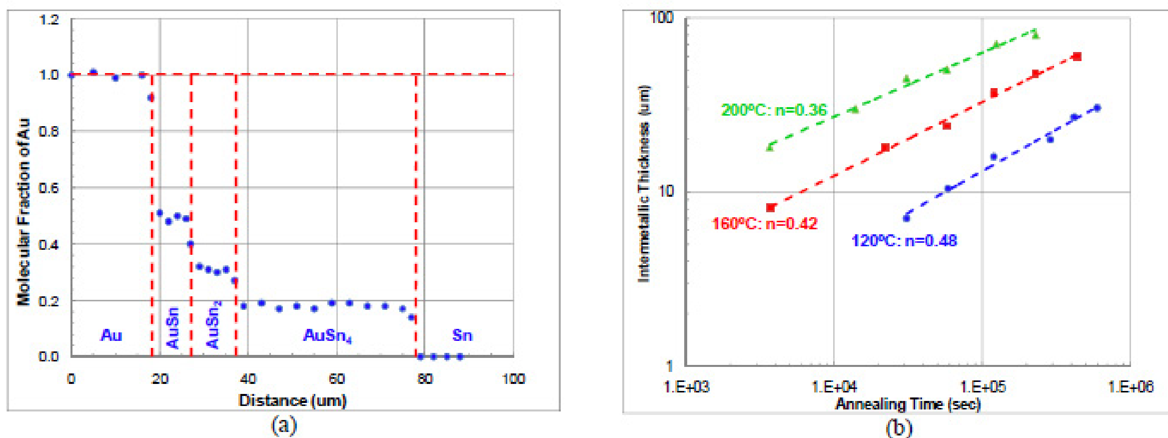

Figure 4: (a) Intermetallic formation in Au-Sn diffusion couple after 127 hrs at 160°C[39]; (b) total intermetallic thickness (AuSn4 + AuSn2 + AuSn) as a function of annealing time at different temperatures, with the associated time exponent in Equation 1[31,39].

/ CONCLUSIONS

This paper provides a review of the critical material and processing issues associated with eutectic AuSn soldering, as well as diffusion rates for multi-layer structures and mechanical behavior. With appropriate design and process development, AuSn solder joints exhibit superior performance in a variety of demanding application environments.

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