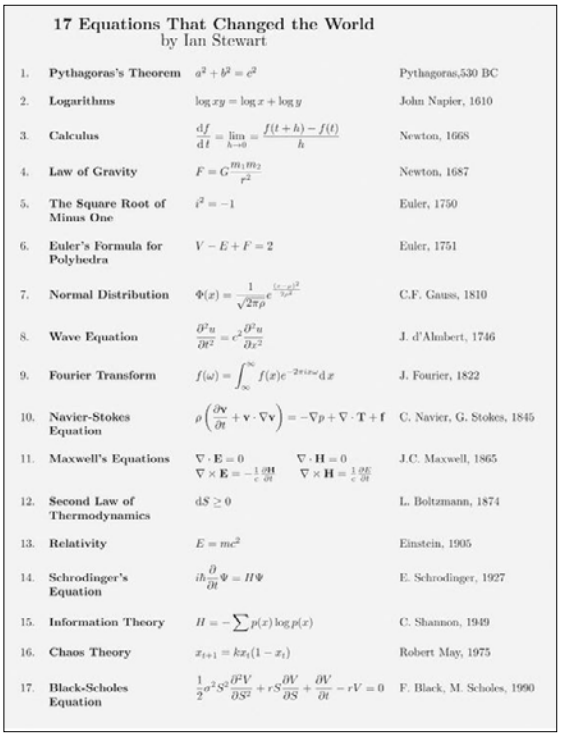
Ansys

17 EQUATIONS THAT CHANGED THE WORLD

Mathematics has been a constant part of our lives forever and is used in many ways in our everyday lives. Created by Ian Stewart, listed on Dr. Paul Coxon's Twitter account, and discussed on mathematics blogger Larry Philip's site is a list of the "17 Equations that Changed the World," many of which have been mentioned on *The Big Bang Theory* TV series.



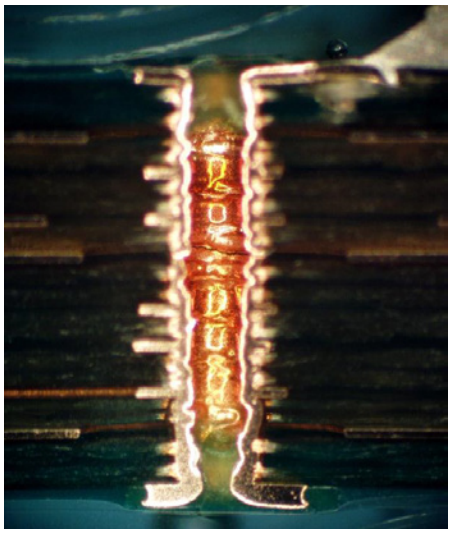
17 Equations That Changed the World
by Ian Stewart

1.	**Pythagoras's Theorem**	$a^2 + b^2 = c^2$	Pythagoras,530 BC
2.	**Logarithms**	$\log xy = \log x + \log y$	John Napier, 1610
3.	**Calculus**	$\frac{df}{dt} = \lim_{h \to 0} = \frac{f(t+h) - f(t)}{h}$	Newton, 1668
4.	**Law of Gravity**	$F = G\frac{m_1 m_2}{r^2}$	Newton, 1687
5.	**The Square Root of Minus One**	$i^2 = -1$	Euler, 1750
6.	**Euler's Formula for Polyhedra**	$V - E + F = 2$	Euler, 1751
7.	**Normal Distribution**	$\Phi(x) = \frac{1}{\sqrt{2\pi}\rho} e^{\frac{(x-\mu)^2}{\gamma^2}}$	C.F. Gauss, 1810
8.	**Wave Equation**	$\frac{\partial^2 u}{\partial t^2} = c^2 \frac{\partial^2 u}{\partial x^2}$	J. d'Alembert, 1746
9.	**Fourier Transform**	$f(\omega) = \int_{\infty}^{\infty} f(x) e^{-2\pi i x \omega} dx$	J. Fourier, 1822
10.	**Navier-Stokes Equation**	$\rho\left(\frac{\partial \mathbf{v}}{\partial t} + \mathbf{v} \cdot \nabla \mathbf{v}\right) = -\nabla p + \nabla \cdot \mathbf{T} + \mathbf{f}$	C. Navier, G. Stokes, 1845
11.	**Maxwell's Equations**	$\nabla \cdot \mathbf{E} = 0$ $\nabla \cdot \mathbf{H} = 0$ $\nabla \times \mathbf{E} = -\frac{1}{c}\frac{\partial \mathbf{H}}{\partial t}$ $\nabla \times \mathbf{H} = \frac{1}{c}\frac{\partial \mathbf{E}}{\partial t}$	J.C. Maxwell, 1865
12.	**Second Law of Thermodynamics**	$dS \geq 0$	L. Boltzmann, 1874
13.	**Relativity**	$E = mc^2$	Einstein, 1905
14.	**Schrodinger's Equation**	$ih\frac{\partial}{\partial t}\Psi = H\Psi$	E. Schrodinger, 1927
15.	**Information Theory**	$H = -\sum p(x) \log p(x)$	C. Shannon, 1949
16.	**Chaos Theory**	$x_{t+1} = kx_t(1 - x_t)$	Robert May, 1975
17.	**Black-Scholes Equation**	$\frac{1}{2}\sigma^2 S^2 \frac{\partial^2 V}{\partial S^2} + rS\frac{\partial V}{\partial S} + \frac{\partial V}{\partial t} - rV = 0$	F. Black, M. Scholes, 1990

However, the list is incomplete. There are numerous equations that help to determine the reliability of electronics products that Ansys believes should be included. These formulas are all integral to the Ansys Sherlock software and are the basis for the validation of the results obtained in an ADA analysis. Let's take a look at them.

/ PLATED THROUGH HOLE FATIGUE

Plated through holes (PTHs), also known as plated through vias (PTVs), are holes drilled through multilayer printed circuit boards (PCBs) that are electrochemically plated with a conductive metal (typically copper). These plated holes provide electrical connections between layers.



Because these plated holes are metallurgically bonded to annular rings on the top and bottom of the PCB, they act like rivets and constrain the PCB. This constraint subjects the PTH to stresses when the PCB experiences changes in temperature.

PTH fatigue is the circumferential cracking of PTHs due to the differential expansion between the copper plating (~17 ppm) and the out-of-plane coefficient of thermal expansion (CTE) of the printed board (~45 to 70 ppm) during temperature variations. This failure mechanism was first reported by Bell Laboratories in 1976.

What are the drivers for PTH fatigue?
PTH fatigue is influenced by maximum temperature, minimum temperature, PTH diameter, PTH copper plating thickness, copper plating material properties (ductility, yield strength), printed board thickness, printed board out-of plane material properties (CTE, elastic modulus), and defects within the copper plating (voids, folds, etch pits, etc.).

How does the software assess PTH fatigue?

The software calculates a time to failure using the industry-accepted model published in IPC-TR-579, "Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in Printed Wiring Boards." Life calculation for PTHs subjected to thermal cycling is a three-step process. The first step is to calculate the stress being experienced by the copper barrel of the PTH. This is provided by the equations below, where α is coefficient of thermal expansion (CTE), T is temperature, E is elastic modules, h is the board thickness, d is the hole diameter, t is the plating thickness, and E and Cu correspond to board and copper properties, respectively.

$$\sigma = \frac{(\alpha_E - \alpha_{Cu})\Delta T A_E E_E E_{Cu}}{A_E E_E + A_{Cu} E_{Cu}}, \text{for } \sigma \le S_y$$

$$\sigma = \frac{\left[(\alpha_E - \alpha_{Cu})\Delta T + S_y \frac{E_{Cu} - E'_{Cu}}{E_{Cu} E'_{Cu}}\right] A_E E_E E'_{Cu}}{A_E E_E + A_{Cu} E'_{Cu}}, \text{for } \sigma > S_y$$

$$A_E = \frac{\pi}{4}\left[(h + d)^2 - d^2\right]$$

$$A_{Cu} = \frac{\pi}{4}\left[d^2 - (d - 2t)^2\right]$$

Once the stress is determined, the strain range is calculated by the following, where Sy is the yield strength of copper:

$$\Delta\varepsilon = \frac{\sigma}{E_{Cu}}, \text{for } \sigma < S_y$$

$$\Delta\varepsilon = \frac{S_y}{E_{Cu}} + \frac{\sigma - S_y}{E'_{Cu}}, \text{for } \sigma > S_y$$

This strain is adjusted by two constants: a strain distribution (Kd) factor and a quality factor (KQ).

$$\Delta\varepsilon_{eff} = \Delta\varepsilon\left(K_d \frac{10}{K_Q}\right)$$

While the strain distribution factor tends to be set to a value of 1.6, KQ is dependent upon the quality of the PTH (i.e., the presence of defects such as voids, cracks, folds, etc.). The quality factor can range from 0 to 10 with the following delineations:

- Extraordinary (KQ = 10)
- Superior (KQ = 8.7)
- Good (KQ = 6.7)
- Marginal (KQ = 4.8)
- Poor (KQ = 3.5)

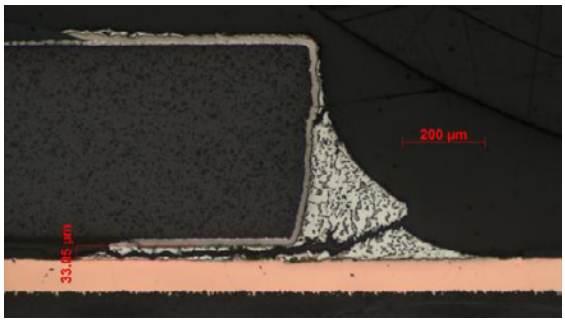
Once the strain range is defined, the cycles to failure (Nf) can be calculated iteratively, with Su being the ultimate tensile strength and Df being ductility of the plated copper.

$$N_f^{-0.6} D_f^{0.75} + 0.9\frac{S_u}{E}\left[\frac{\exp(D_f)}{0.36}\right]^{0.1785\log\frac{10^5}{N_f}} - \Delta\varepsilon = 0$$

Reviewing the equations above, it can be seen that the designer and PCB manufacturer have the following controls over the reliability of PTHs:

- Out-of-plane CTE of the printed board
- Plating thickness
- Aspect ratio (hole diameter over board thickness)
- Plating material properties (i.e. strength and ductility) and plating quality

/ THERMO-MECHANICAL SOLDER JOINT FATIGUE?



Solder joints, also known as interconnects, provide electrical, thermal, and mechanical connections between electronic components (passive, discrete, and integrated) and the substrate or board to which it is attached. Solder joints can be a first-level (die to substrate) or second-level (component package to printed board) connection. This module assesses the thermo-mechanical fatigue behavior of second-level solder joints.

During changes in temperature, the component and printed board will expand or contract by dissimilar amounts due to differences in the CTE. This difference in expansion or contraction will place the second-level solder joint under a shear load. This load, or stress, is typically far below the strength of the solder joint. However, repeated exposure to temperature changes, such as power on/off or diurnal cycles, can introduce damage into the bulk solder. With each additional temperature cycle, this damage accumulates, leading to crack propagation and eventual failure of the solder joint.

The failure of solder joints due to thermo-mechanical fatigue is one of the primary wearout mechanisms in electronic products, primarily because inappropriate design, material selection, and use environments can result in relatively short times to failure.

What are the drivers for thermo-mechanical solder joint fatigue?
Thermo-mechanical solder joint fatigue is influenced by maximum temperature, minimum temperature, dwell time at maximum temperature, component design (size, number of I/O, etc.), component material properties (CTE, elastic modulus, etc.), solder joint geometry (size and shape), solder joint material (SnPb, SAC305, etc.), printed board thickness, and printed board in-plane material properties (CTE, elastic modulus).

How does the software assess thermo-mechanical solder fatigue?
The software calculates time to failure using strain energy. The detailed methodology is provided by the equations below. The first equation describes the force exerted on a solder joint during a thermal cycle:

$$(\alpha_2-\alpha_1)\cdot\Delta T\cdot L_D = F\cdot\left(\frac{L_D}{E_1A_1}+\frac{L_D}{E_2A_2}+\frac{h_s}{A_sG_s}+\frac{h_c}{A_cG_c}+\left(\frac{2-\nu}{9\cdot G_b a}\right)\right)$$

In this equation, α is the CTE, T is temperature, L is one half component length, F is force, E is elastic modulus, A is the effective solder joint area, G is the shear modulus, h is thickness, and ν is the Poisson ratio. The strain range induced in the solder joint during the thermal cycle is.

$$\Delta\gamma = \frac{L_D}{h_s}\Delta\alpha\Delta T\cdot\left(\frac{D_{dwell}}{360}\right)\cdot e^{\left(2189\left(\frac{1}{398}-\frac{1}{T_{max}}\right)\right)}$$

The equations above are package-specific and account for the geometry, interconnect structure, and material properties of the component and PCB. The stress on the solder joint is determined using the computed forces, and this stress is combined with the strain to determine the energy dissipated by the solder during a thermal cycle through the equation (see right).

$$\Delta W = 0.5\cdot\Delta\gamma\cdot\frac{F}{A_s}$$

The resulting strain energy is used to compute the number of cycles to failure for the component under temperature cycling using equations developed by Syed (see right).

Sn3Ag0.5Cu -- $N_f = (0.0019\cdot\Delta W)^{-1}$

63Sn37Pb -- $N_f = (0.0006061\cdot\Delta W)^{-1}$

/ WHAT IS THE SHOCK AND VIBRATION MODULE?

The Shock/Vibration module in Ansys Sherlock utilizes the finite element method to predict the circuit card assembly (CCA) response during mechanical shock and harmonic or random vibration events. The board response results are then used to make predictions on the robustness of the CCA to these events. In the case of vibration, high cycle fatigue predictions are made to determine the life of the interconnect (lead and solder joint). The shock analysis results are used to determine if a critical stress due to board bending is exceeded.

Second-level interconnects provide electrical, thermal, and mechanical connections between electronic components (passive, discrete, and integrated) and the substrate or board to which it is attached. The vibration portion of the module assesses the high cycle fatigue behavior of second-level interconnects.

How does the software assess vibration?
During exposure to vibration, the CCA responds by cyclic deflecting in a manner that corresponds to its natural frequencies. These natural frequencies are dependent on the geometry, stiffness, mass, and boundary conditions of the CCA. The software automatically generates the model and then utilizes the open-source finite element analysis (FEA) engine CalculiX to conduct the shock and vibration response shows the vibration analysis of a circuit board using CalculiX. The CalculiX FEA analysis engine was originally developed by Guido Dhondt and is open source covered under GNU General Public License. The naming conventions and input style formats for CalculiX are based on those used by ABAQUS, a proprietary, general-purpose finite element code developed and supported by Hibbitt, Karlsson & Sorensen, Inc. (HKS).

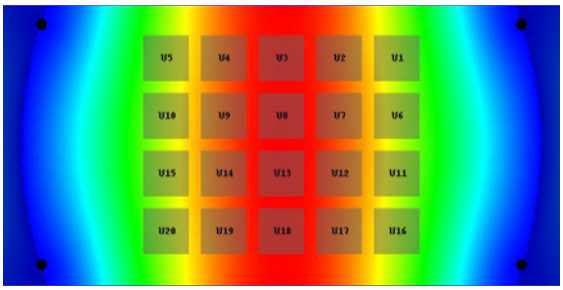


Figure 1. Ansys Sherlock finite element analysis (FEA) output showing a vibration analysis of a circuit board

The software generates a three-layer shell model of the circuit card assembly with six-node triangular elements that define the top components, bottom components, and printed wiring board. These six-node shell elements are expanded into 15-node three-dimensional wedge elements automatically by CalculiX during analysis.

The output of the FEA is post-processed by the software, and the maximum board level strains for every component are recorded for use in determining whether that component fails during exposure to the shock and vibration loads. There are four types of vibration analyses that the software conducts:

1. Natural frequency extraction
2. Single-point harmonic vibration
3. Swept harmonic vibration
4. Random vibration

The first analysis, natural frequency extraction, is used to extract the fundamental frequencies of the circuit card assembly.

/ HOW DOES THE SOFTWARE ASSESS VIBRATION FATIGUE USING BOARD STRAINS?

The failure of solder joints due to vibration is based upon a technique similar to the one developed by Steinberg. The main modification is converting from a displacement-based criteria to a board-level strain criteria. The Steinberg critical PCB deflection, at which a component will survive 10 million cycles during harmonic vibration or 20 million cycles during random vibration, is:

$$Z_c = \frac{0.00022B}{chr\sqrt{L}}$$

Where:
B is length of PCB parallel to component
c is a component packaging constant (typically between 0.75 and 2.25)
h is the PCB thickness
r is a relative position factor and is 1.0 when component is located at the center of the PCB
L is component length

The main issue with this approach is that it is limited to simple board geometries (since the maximum deflection is always assumed to be at the center of the PCB) and doesn't account for board curvature. By utilizing finite element modeling, the software eliminates some of the variables in the equation since they are accounted for in the FEA model. These include board length (B), position factor (r), and board thickness (h), and the equation is simplified to:

$$\varepsilon_c = \frac{\zeta}{c\sqrt{L}}$$

ζ is analogous to 0.00022B (B is the edge length of the PCB) but represents strain
c is a component packaging constant (typically between 0.75 and 2.25)
L is component length

The software uses this critical strain value and the FEA-computed strain values to make fatigue predictions using the Basquin equation:

$$N_{FEA} = N_c\left(\frac{\varepsilon_c}{\varepsilon_{FEA}}\right)^b$$

Where:
NFEA is the predicted number of cycles to failure
Nc is 10E6 for harmonic of 20E6 for random vibration
εc is the critical strain value and is a function of component type and size
εFEA is maximum printed circuit board strain recorded at the component
b is the fatigue exponent and is dependent on the solder alloy

Currently, the software does not make fatigue predictions based on a mechanical shock loading. Mechanical shock is instead viewed as an overstress event and is based on exceeding a predefined board level strain. This analysis is an extension to the type of information provided in IPC-9704 for ball grid array (BGA) devices. The software utilizes these limits as the generic values for all components.

If the strain level anywhere at the parts locations exceeds the acceptable amount, the part is considered to fail the shock robustness portion of the analysis. Figure 3 shows plot of Maximum allowable principal strain vs. strain rate for circuit boards with variable thickness. The shock analysis utilizes the CalculiX-based FEA to determine the circuit card assembly's response and the part-level strains that occur during the shock event.

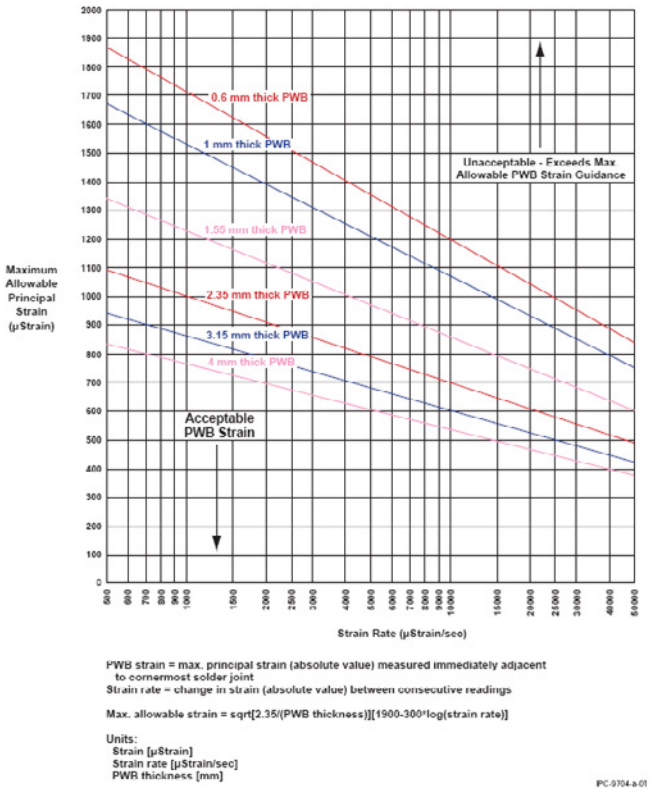


Figure 3. Plot of maximum allowable principal strain vs. strain rate

/ WHAT IS THE COEFFICIENT OF THERMAL EXPANSION?

Almost all materials exhibit a change in physical dimensions when subjected to temperature changes. The degree of expansion in response to a change in temperature is called the coefficient of thermal expansion (CTE).

CTE is critical because when two materials with different CTE are joined, a stress is imparted because of the resultant displacement mismatch. This is the main driver of thermal-mechanical fatigue of electronic components.

During changes in temperature, the component and printed board will expand or contract by dissimilar amounts due to differences in the CTE.

This difference in expansion or contraction will place the second-level solder joint under a shear load. This load, or stress, is typically far below the strength of the solder joint. However, repeated exposure to temperature changes, such as power on/off or diurnal cycles, can introduce damage into the bulk solder.

The calculation of the CTE of the PCB is critical as input for determining thermo-mechanical fatigue of solder interconnects.

How is the PCB CTE calculated?
The Sherlock software uses lamina theory for calculating the CTE of PCB. PCBs are composed of alternating layers of glass-reinforced epoxy laminate/prepreg and copper foil.

The mechanical properties of the laminate and copper foil are:
- Coefficient of thermal expansion, in plane (CTExy)
- Coefficient of thermal expansion, out of plane (CTEz)
- Elastic modulus, in plane (Exy)
- Elastic modulus, out of plane (Ez)

The stackup tool allows the copper thicknesses to be in ounces/milliliters/microns, where 1 oz = 35 microns = 1.4 mil.

Term definitions
- CTExypcb is the coefficient of thermal expansion, in-plane of the PCB
- CTEzpcb is the coefficient of thermal expansion, out of plane of the PCB
- Exypcb is the elastic modulus, in plane of the PCB
- Ezpcb is the elastic modulus, out of plane of the PCB
- CTExyln is the coefficient of thermal expansion, in-plane of layer n (the first and last layer will always be copper)

- CTEzln is the coefficient of thermal expansion, out of plane of layer n
- Exyln is the elastic modulus, in-plane of layer n
- Ezln is the elastic modulus, out of plane of layer n
- tln is the thickness of layer n
- tpcb is the overall thickness of the PCB

Calculating mechanical properties of the printed circuit board takes the general forms below.

$$1/CTExypcb = \left[\left(\frac{tl1}{tpcb}\right)/CTExyl1\right] + \left[\left(\frac{tl2}{tpcb}\right)/CTExyl2\right] + \ldots + \left[\left(\frac{t\ln}{tpcb}\right)/CTExy\ln\right]$$

$$CTEzpcb = \left[CTEzl1 \times \left(\frac{tl1}{tpcb}\right)\right] + \left[CTExyl2 \times \left(\frac{tl2}{tpcb}\right)\right] + \ldots + \left[CTExy\ln \times \left(\frac{t\ln}{tpcb}\right)\right]$$

$$Exypcb = \left[Exyl1 \times \left(\frac{tl1}{tpcb}\right)\right] + \left[Exyl2 \times \left(\frac{tl2}{tpcb}\right)\right] + \ldots + \left[Exy\ln \times \left(\frac{t\ln}{tpcb}\right)\right] \text{ (Voigt composite)}$$

$$1/Ezpcb = \left[\left(\frac{tl1}{tpcb}\right)/Exl1\right] + \left[\left(\frac{tl2}{tpcb}\right)/Exyl2\right] + \ldots + \left[\left(\frac{t\ln}{tpcb}\right)/Exy\ln\right] \text{ (Reuss composite)}$$

The copper layers are computed assuming a combination of copper and unreinforced resin rich regions. This is a critical aspect of the CTE calculation, especially when the copper weight increases above 2 oz.

This is just the beginning of the validation formulas that are integral to Sherlock. In a future white paper, Ansys will address flex cracking of components, cyclic bending, conductive anodic filament (CAF), and interconnect (IC) wearout.

So, as previously stated, there are numerous equations that provide reliability validation. Look for the second white paper to illustrate the rest that are currently in Ansys Sherlock and provide the basis for a physics of failure (PoF) approach to reliability assessments.

For more information, and to request a quote from our Ansys Reliability Engineering Services Team, visit: https://upl.inc/a5b0679

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