Safe Travels

AUTOMOTIVE ELECTRONICS have always had to withstand difficult environment conditions. Today, with the safety of the vehicle's occupants increasingly dependent on these same electronics, the consequences of failure are greater than ever before. Engineering simulation is essential to diagnose and validate automotive electronics reliability before investing in expensive prototypes and field testing.
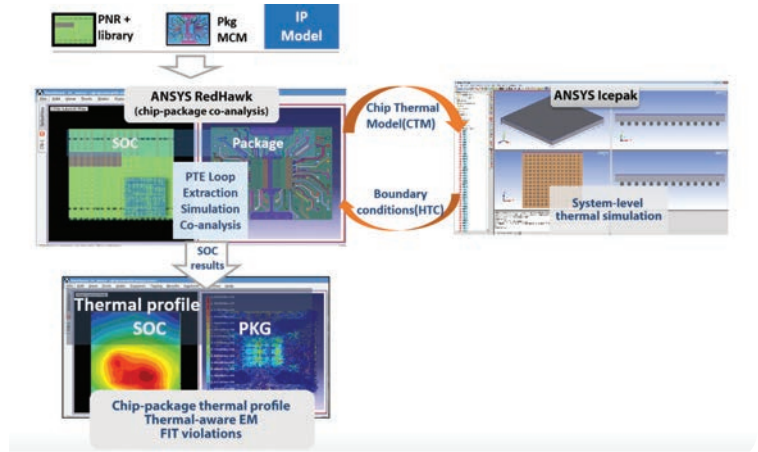
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As automotive electronics' role transitions from entertaining the driver to assisting the driver, to taking full control of the vehicle, its reliability is coming under increasing scrutiny. Critical automotive electronic systems need to last more than 10 years, often under hostile underhood environments where temperatures can range up to 150 C. ANSYS simulation tools enable engineers to simulate, debug and optimize proposed electronic systems designs with respect to issues that might cause an automated driving system to fail. Simulation makes it possible to design robust and efficient electronic systems that meet demanding reliability requirements for autonomous driving applications. This article will focus on the varied aspects of reliability and chip–package–system (CPS) simulations that enable package/system-aware integrated circuit (IC) design and IC-aware package/system design.

Autonomous Driving Reliability Challenges

Today's drivers increasingly depend upon electronic systems to ensure safety. For example, nearly every car uses an anti-lock braking system to reduce stopping distance in slippery conditions. The recent proliferation of advanced driver assistance systems (ADAS) capabilities, such as applying the brakes automatically if the vehicle ahead stops or slows suddenly, have further increased the importance of electronics in vehicle safety. Of course, the emergence of autonomous driving systems that understand every conceivable driving situation and make judgments to ensure the safety of vehicle occupants and pedestrians will further increase the dependence of driver, passenger and pedestrian safety on automotive electronics.

ANSYS chip–package–system thermal reliability analysis with ANSYS RedHawk-CTA and ANSYS Icepak

Many current automotive electronics applications reside on semiconductors based on older process nodes that are relatively easy to validate from a reliability standpoint because of their large feature size and the experience of designers. However, the sensors used in ADAS and autonomous driving technology generate
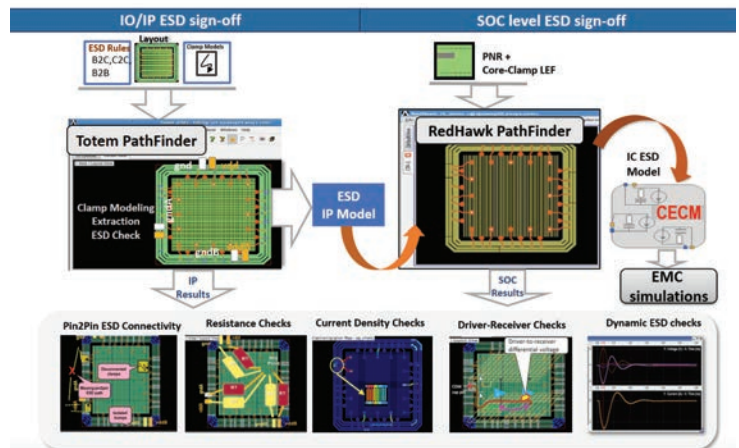
> "*Simulation makes it possible to design robust and efficient electronic systems that meet demanding reliability requirements for autonomous driving applications.*"

huge amounts of data (40 gigabytes per hour is not unusual) that must be processed at blinding speeds and with low latency. These applications require vast increases in computing power that can be satisfied only by leading-edge semiconductor processes with much smaller feature sizes that are just now reaching the market.

The new generation of integrated circuits, designed in advanced process nodes, pack more transistors into a smaller footprint to deliver the highest possible levels of computing performance. These ICs operate at much lower supply voltages, making them more susceptible to power and signal noise coupling. Another

ANSYS PathFinder ESD/EMC workflow

challenge is that in many cases these semiconductors will need to operate in underhood environments where ambient temperatures can reach up to 135 C, which makes them more susceptible to thermal-induced failures. This thermal challenge is intensified because electronic components in many automotive applications are exposed to water and dirt, so they must be sealed against the elements. This increases the difficulty of providing adequate cooling.
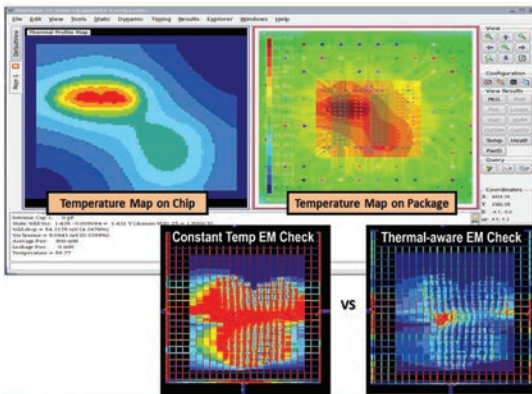
"*The ability to identify and troubleshoot reliability issues with simulation makes it possible to achieve substantial reductions in time to market and to improve reliability.*"

Electromigration

The proliferation of automotive semiconductors based on leading-edge process nodes that enable ADAS and autonomous driving makes electromigration — a lifetime reliability problem — a critical system design issue. Electromigration (EM) occurs when electrons flow through an integrated circuit and collide with the metal atoms in the conductors and gradually create an open or a short. Over time, this causes the chip to fail. Chips become more susceptible to EM as their conductor cross section shrinks at each successive process node. EM also exponentially increases as a function of temperature. Advanced 2.5D and 3D integrated circuits are bringing dies closer together, creating the potential for more thermal hot spots.

Typically, the temperature of the individual conductors on a chip is not known, so design engineers assume a uniform worst-case temperature across the chip. This approach was satisfactory at older process nodes, but the faster switching speeds, narrower conductors and higher number of layers within today's advanced process nodes greatly increase the number of EM violations when this approach is used. Design teams spend increasing amounts of time evaluating and fixing these violations, many of which are false and would never have been triggered if the simulation had been based on an accurate nonuniform temperature profile.

The ANSYS RedHawk platform addresses these challenges by accurately determining the increase in temperature around the devices and metals to accurately predict EM violations. This increase in temperature is modeled using the Joule self-heat and thermal coupling principles between metal conductors inside a chip. The device temperature is a function of the amount of current consumed by each transistor as well as the proximity to neighboring transistors. Process parameters from the foundry combined with thermal characteristics of the metals and dielectrics used on the die are used to accurately predict the localized temperature changes.
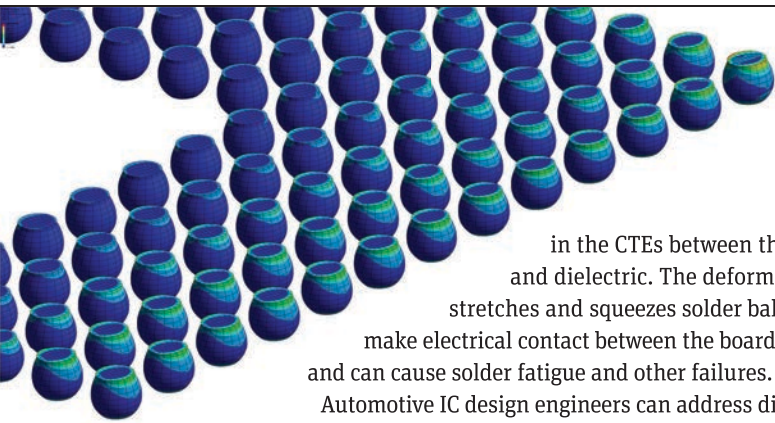
The temperature profile is used to perform thermal-aware EM checks based on the actual temperatures experienced by each wire on the chip. This approach greatly reduces the number of EM violations while providing much more diagnostic information than was available in the past to aid in addressing them. Engineers can zero in on the EM violations that really matter and can fix these violations faster. The result is a significant reduction in time to market and a lower risk of EM failure.

Thermal analysis of chip and package using ANSYS RedHawk-CTA
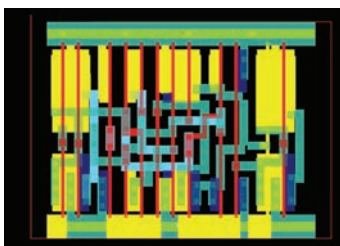
Wire temperatures used to calculate thermal-aware electromigration

Thermal Performance

Thermal effects are another major concern in ensuring the reliability of critical automotive semiconductors. At the die and package level, engineers need to ensure that the temperatures across the chip do not exceed maximum operating temperatures at any point. Furthermore, they must evaluate thermal cycles during operation that generate deformation on the die and package because of differences in the coefficients of thermal expansion (CTEs) between the wafer and the metal layer. Thermal cycles at the board level can also generate stress due to differences

in the CTEs between the copper and dielectric. The deformation stretches and squeezes solder balls that make electrical contact between the board and chip, and can cause solder fatigue and other failures.

Automotive IC design engineers can address die-level thermal reliability issues using ANSYS chip thermal models (CTMs) to solve for a complete chip-and-package co-analysis. The temperature profiles from the analysis can then be used inside ANSYS Mechanical to predict the impact of temperature on stress, strain and deformations generated by thermal or mechanical loading on the die. At the board level, the ANSYS SIwave signal integrity analyzer can be used to compute Joule heating in printed circuit board (PCB) traces and vias to create a board trace map and current density predictions. This is exported to the ANSYS Icepak systems-level thermal simulation tool, which calculates the orthotropic thermal conductivity of the PCB and temperatures at every point in the solution domain. These temperatures are transferred back to SIwave to update the electrical properties of the board based on the temperature field. SIwave and Icepak then iterate until the temperatures converge. The temperatures are used to load a structural model of the board and predict stresses and deformations.
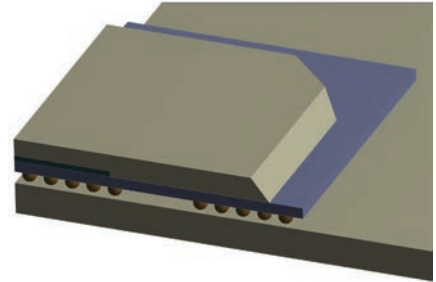
Electrostatic Discharge

The smaller feature sizes and isolated and independent power/ground networks often found in advanced process nodes increase the risk of electrostatic discharge (ESD) failures. The traditional approach to ESD verification involves following engineering guidelines in creating the layout and running design rule checks. But these methods cannot predict if the overall resistance and current density of the ESD paths are below the threshold limit.

ANSYS PathFinder uses block-level static and dynamic techniques as well as full-chip level static methods to identify weak areas in the design and determine whether or not it meets ESD guidelines. PathFinder verifies the effective resistance between any two pads/bumps traversing the network through a clamp cell; between pads/bumps to every connecting clamp cell; between multiple clamp cells; and between active devices and clamp cells for pass/fail checks. PathFinder estimates the effective resistance from the devices in the IC to the clamp cells that are inserted to provide a discharge path. PathFinder highlights the wire/vias that fail the current density limits, allowing the designers to verify that the current flow during a discharge event is within the established limits defined by technology or process guidelines.

The safety of ADAS and autonomous driving systems is only as good as the reliability of the electronic systems they run on. ANSYS simulation tools enable engineers to perform EM analysis based on the temperature experienced by each wire on the chip. This approach saves time by highlighting the truly problematic traces. ANSYS thermal simulation tools further enable engineers to evaluate the complete thermal ecosystems to identify and correct thermal problems at the die, package, board and system level. Finally, ANSYS simulation tools enable engineers to identify and troubleshoot ESD problems. The ability to identify and troubleshoot reliability issues with simulation enables companies to ensure the reliability of ADAS and autonomous driving electronics in a rigorous yet efficient fashion, making it possible to achieve substantial reductions in time to market and improving reliability. ⚠

Fast Tracking ADAS Autonomous Vehicle Development with Simulation
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