ENSURING ELECTROMAGNETIC COMPATIBILITY

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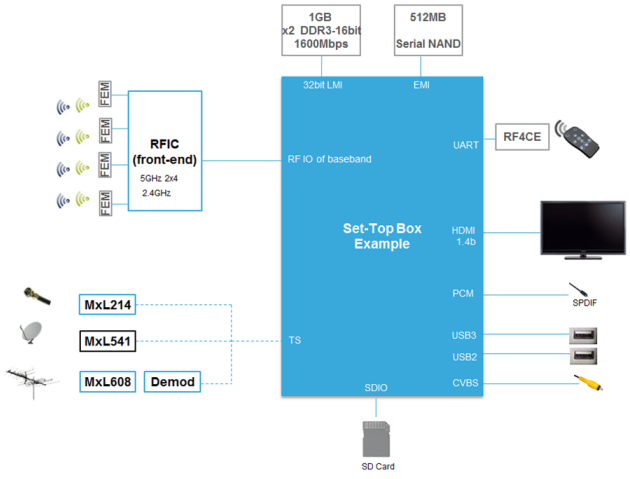
STMicroelectronics has developed a workflow that combines full-wave frequency domain with circuit simulation to determine electromagnetic interference / electromagnetic compatibility and electromagnetic coexistence issues before physical prototyping. The new approach has been proven to identify and fix, early in the design process, issues that could otherwise delay the product launch by up to four months or 20 percent of the development time.

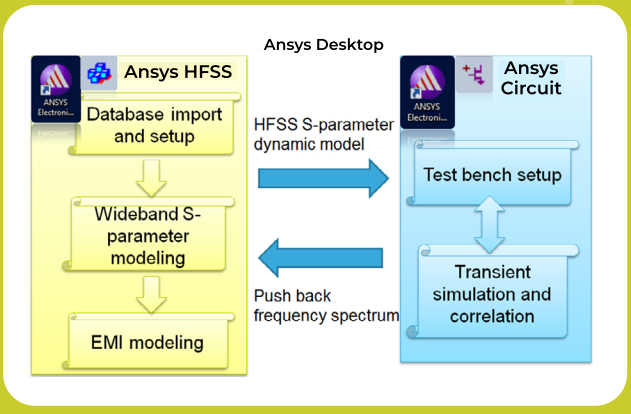
The dramatic proliferation of wireless (Wi-Fi, Bluetooth, ZigBee, etc.) and wired communications channels, combined with higher data rates and increasing package density, has greatly increased the challenges involved in achieving compliance with electromagnetic interference (EMI) / electromagnetic compatibility (EMC) standards that have been developed to avoid interference between coexisting interfaces. Traditionally, these issues are addressed during the design process using an electromagnetic simulator to extract an S-parameter model of individual features that are expected to create difficulties. This approach has limited accuracy because the S-parameter model is usually excited with a generic signal, so electrical and magnetic emissions predicted by full-wave simulation may differ significantly from the actual circuit.



Set-top box used to validate new simulation methodology

"Improved *EM simulation techniques* and large-scale HPC empower engineers to simulate the entire PCB with *full-wave accuracy*."

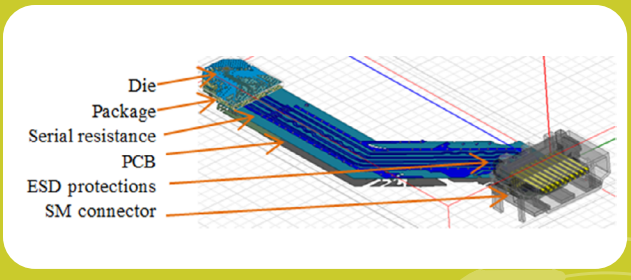
Engineers at STMicroelectronics, a global semiconductor company with innovative semiconductor solutions for autonomous vehicles and the Internet of Things, address this challenge using a workflow based on the Ansys HFSS 3-D finite element model (FEM) electromagnetic (EM) solver to model the structure and calculate EM fields in the frequency domain. Leveraging the Ansys Electronics Desktop environment, the resulting S-parameter model is embedded in the circuit model. The HFSS circuit analyzer provides a realistic excitation of the HFSS model to accurately predict the magnetic and electrical emissions of the actual circuit. Simulation results generated using this approach correlate well with experimental measurements, so it can be used with confidence to identify EMI and coexistence problems and evaluate potential mitigation techniques. Ansys tools make it possible to rapidly deliver robust EMI/EMC-compliant products.



Simulation workflow used to generate realistic excitation for full-wave model

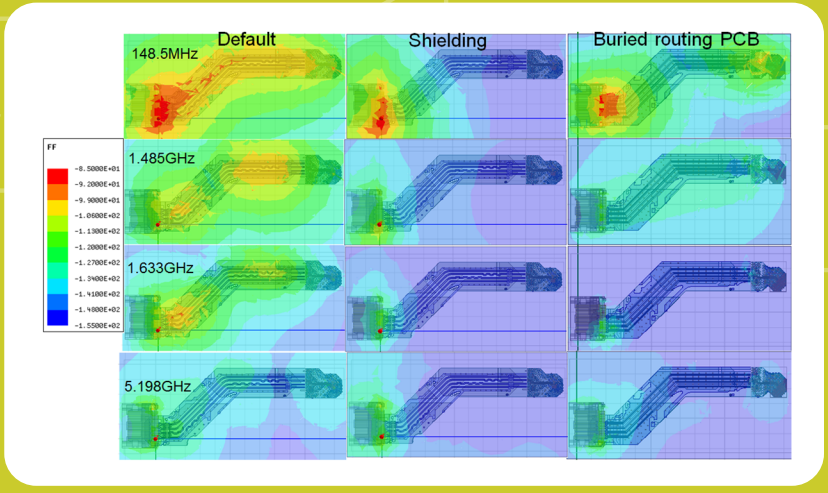
Ensuring EMI/EMC Compliance

No aspect of modern electronics design presents greater difficulties than ensuring the proper coexistence of the many digital interfaces found in today's cutting-edge electronics products, such as mobile phones, set-top boxes and wearables. The challenge is to ensure that each individual interface in a complete system delivers the same level of performance as it would in isolation. Current simulation methods address individual interactions, such as the determination of whether the double data rate synchronous dynamic random-access memory (DDR SDRAM) interferes with the USB3.1. But today's leading-edge products often have so many different features that it is almost impossible to know in advance which have the potential to interact in harmful ways. Too often these problems are discovered during testing, which requires a redesign that delays the product launch as the problems are mitigated using trial-and-error methods.



Full-wave model of communications channel

EMI/EMC and Coexistence Simulation for High-Performance Digital, Mixed-Signal and RF Wireless Products
ansys.com/EMI-EMC



Average H-field with default design, shielding and buried routing

Realistic Excitation of Full-Wave Model

Now, the combination of improved EM simulation techniques and large-scale, high-performance computing (HPC) makes it possible to simulate the entire PCB with full-wave accuracy. The methodology developed by STMicroelectronics engineers goes one step further by performing transient simulation using the full-wave model with realistic excitation patterns. Results of the circuit simulation are back-annotated to the full-wave model to reproduce real-world EM fields. This approach was validated on an existing digital high-speed transmission channel in a set-top box and used to evaluate potential EMI/EMC mitigation methods in the simulation space.

The HFSS S-parameter model was converted to a SPICE-like model and linked inside the HFSS circuit environment. The HFSS model remained at a manageable size by defining the appropriate box type and size around the structure, port types, frequency sweep for wideband S-parameter modeling, mesh settings and convergence criteria. The port excitations were set by drivers in IBIS format using a pseudo-random bit sequence

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(PRBS) to reproduce a real use case. The transient simulation generated eye diagrams and H-fields that correlated very well with physical measurements in the time domain. The next step was to push the excitation back into HFSS to recalculate the EM fields, focusing on the magnetic fields that dominate the electrical fields in this case.

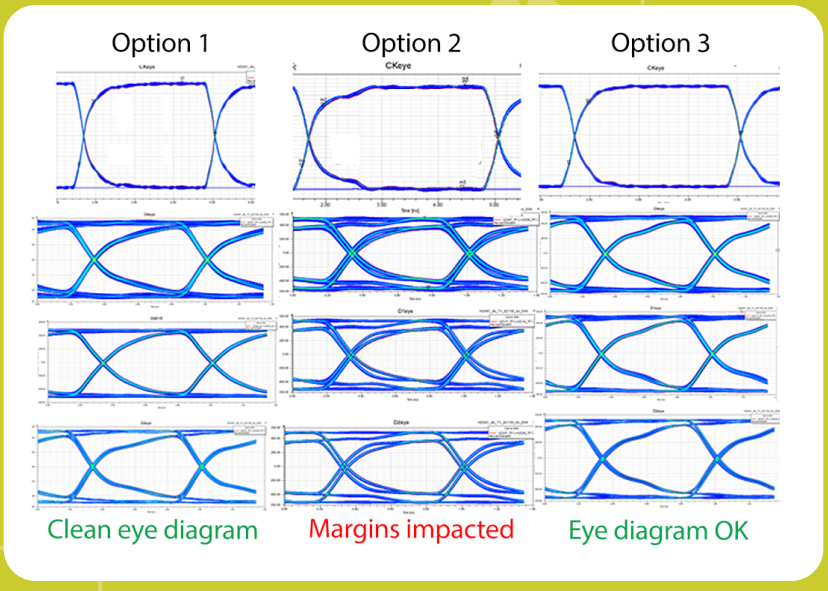
Evaluating Potential Mitigation Methods

STMicroelectronics engineers investigated the use of functional and physical layout techniques to mitigate EMI/EMC risks. Increasing the slew rate from 5 percent to 8 percent of the unit interface (UI) provided an average of 3 dB of mitigation on the clock frequency spectrum, reducing the radiated magnetic field. Engineers also implemented the spread spectrum clock (SSC) method to reduce EMI by up to 10 dB on the third harmonic and 15 dB on the fifth harmonic. They evaluated the effects of

Ansys HFSS: Layout-Driven Assembly in Ansys Electronics Desktop
ansys.com/layout-driven

> **"A new cost-optimized and *EMC-compliant product* can be brought to market and begin generating revenues with much *lower development risk* and shorter design cycle."**

placing common-mode filters at different locations on various harmonics. The results showed that for this design, common-mode filtering using STMicroelectronics ECMF04-4HSWM10 is more efficient when the filter is placed closer to the source of the signals, in this case the system-on-chip (SOC). EMI radiation is reduced by up to 25 dB on even harmonics of the clock. Engineers also evaluated the impact of 1 mm copper shielding with a 10 mm by 0.6 mm aperture and found that the gain on the average H-field rose from 15 dB to 20 dB, except at the shield resonance frequency of 2.4 GHz to 2.5 GHz, where the gain was only about 6 dB. On the other hand, buried PCB routing increased H-field gain from 5 dB to 15 dB, except at the routing resonance, where the radiation gain was only about 0.66 dB.



Eye diagrams of the clock with common mode filtering used at three different locations

The growing integration of high-speed digital communications technologies has increased the difficulty of achieving compliance with EMI/EMC standards and EM coexistence. In many new products, ensuring compliance requires a redesign during the prototype phase, which increases engineering and prototyping costs and delays new product introduction with associated revenue losses. The new methodology developed by STMicroelectronics makes it possible to perform full-wave EM simulation with a realistic excitation. The resulting high level of accuracy provides a way to confidently identify EMI/EMC and coexistence problems and evaluate the relative effectiveness of a wide range of mitigation measures long before a prototype is available. A new cost-optimized and EMC-compliant product can be brought to market and begin generating revenues with much lower development risk and shorter design cycle. ∧

Reference
ECMF components by STMicroelectronics
www.st.com/ecmf

Turning Signal Integrity Simulation Inside Out
ansys.com/signal-integrity