

# Six Steps to Successful Board Level Reliability Testing

As the smartphone market has stagnated — the number of iPhones sold worldwide has not changed in almost four years — semiconductor manufacturers are pivoting their focus to automotive electronics to find the next large volume growth opportunity. This adjustment is for good reason as automotive electronics are projected to be the fastest growing market for integrated circuits until at least 2021.

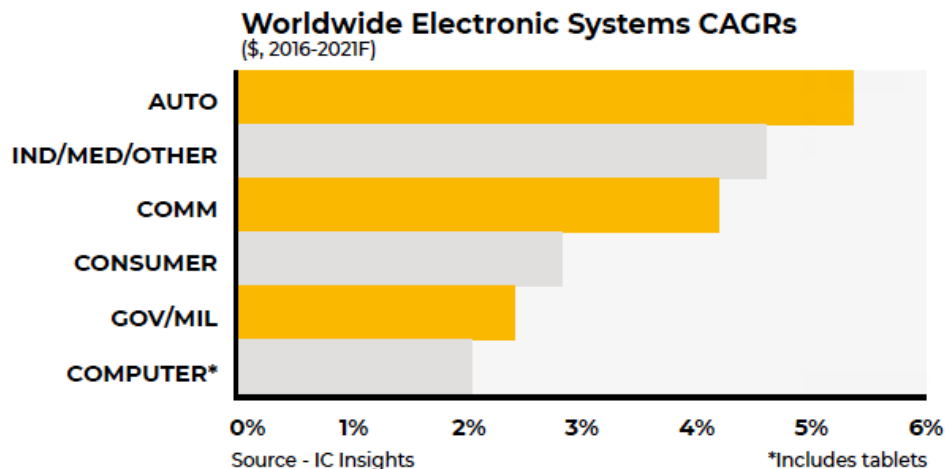
To be successful in the competitive automotive electronics landscape, semiconductor manufacturers must account for differences in how automotive OEMs and their suppliers qualify integrated circuits compared to consumer products. While the differences are numerous, a key factor is the critical importance of board level reliability testing (BLRT).

This white paper is designed to provide semiconductor companies — including manufacturers of multi-chip modules (MCM) and system-in-package (SiP) — clear insight into the six steps necessary to have a meaningful and successful plan for performing BLRT on a device.

## / 1. What is BLRT?

BLRT is the process of evaluating the robustness of a semiconductor package once the device is soldered to the printed circuit board (PCB). The primary focus of BLRT has been on the reliability of the solder joint but there are other aspects of the semiconductor package which are susceptible to failure only after assembly. BLRT, while relatively common now, was a deviation from common semiconductor qualification practices. Legacy requirements, beginning with the military standard MIL-STD-883, mainly focused on the robustness of the standalone device. All testing (temp cycling, mechanical shock, humidity, etc.) was performed without permanently attaching the device to anything. The semiconductor industry considered performing BLRT as part of a standard qualification process following failures in ball grid array (BGA) and quad-flat no leads (QFN) packaging along with several other high-profile solder disappointments, with cyclic bending failure under cellphone keypads being the most frequent.

There is no better example than the qualification documents created by the Automotive Electronics Council (AEC). The AEC is effectively considered the component standards body for the automotive industry and therefore develops templates for qualifying integrated circuits (Q100), discretives (Q101), passives (Q200) and multi-chip modules (Q104). Unfortunately, only Q104 discusses how BLRT qualifies devices for automotive applications but provides only limited guidance on test parameter and duration requirements. This results in costly surprises for automotive Tier 1 manufacturers when they perform their board or system-level qualifications tests.



## / 2. How to Perform BLRT

Despite the lack of standardization, there are industry documents that can help develop individual BLRT tests. The most overarching document is “Stress-Test Driven Qualification of and Failure Mechanisms Associated with Assembled Solid-State Surface Mount Components (JEDEC JEP150).” Initially released in 2005 and then updated in 2013, the document provides a table of potential BLRT tests and helpful standards for developing these tests. A pared-down list of recommended BLRT tests (some tests are considered optional) is shown opposite:

Assembly to the board:	Per JESD22A113
Temperature/Humidity/Bias (THB):	No test standard provided
Temperature/Humidity:	No test standard provided
Temperature Cycling:	Per JESD22A104, Condition J
Power Temperature Cycling:	Per JESD22A105
Drop Testing:	Per JESD22B110, Condition A
Vibration, Harmonic:	Per JESD22B103, Condition 1
Bending, Monotonic and Cyclic:	Per IPC/JEDEC 9702

AEC Q104 also provides a list of the following recommended BLRT but less than those provided in JEP150:

Temperature Cycling:	Per IPC-9701
Low Temperature Storage Life: :	Per JESD22A119
Start Up and Temperature Steps:	Per ISO 16750-4
Drop Testing:	Per JESD22B111, Condition B

Other examples of industry standards that describe BLRT include IPC-9703 Mechanical Shock, IPC-9707 Spherical Bend and JESD22B113 Cyclic Bend. These standards generally omit clear guidance regarding test coupon design, test conditions, test duration and definition of failures.

This vagueness can be considered an advantage, providing flexibility to the semiconductor manufacturer in helping them pass BLRT qualification.

Conversely, it can be considered a disadvantage when a customer makes certain assumptions regarding BLRT that are not valid.

The lack of a universal standard for BLRT results in confusion, delay and dissatisfaction up and down the supply chain.

## / 3. Developing a BLRT Plan

The first step in developing a BLRT plan is identifying which tests to include. The most important test to include in BLRT is temperature cycling because:

- It is one of the most common environments across potential customers, second only to constant temperature. Far fewer customers experience excessive humidity, vibration or mechanical shock.
- It is the stress most likely to cause failure of BGA and QFN solder joints.
- It is the longest and most expensive qualification test performed by Tier 1 manufacturers and OEMs.
- There have been several industry-wide issues regarding package failures that only occur when temperature cycling assembled parts. These issues include copper wire bond failures and low-K dielectric cracking (also known as chip-package-board interaction).

Choosing a specific standard for temperature cycling, such as JESD22A105 or IPC-9701, is not critical unless a customer requires it. The most important aspects are selecting the minimum temperature, the maximum temperature, the number of temperature cycles and the test coupon design. Common test parameter selection mistakes include:

<p><b>1</b> Assuming the minimum and maximum test temperature should be the same as the minimum and maximum rated temperature.</p>	<p><b>2</b> Choosing something other than 1,000 cycles — this makes customers nervous.</p>	<p><b>3</b> Failing to take full advantage of the test coupon design to reduce risk, pass BLRT and streamline customer acceptance.</p>
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Other potential BLRT tests — power cycling, temperature/humidity, mechanical shock, vibration and bend testing — depend on finding the appropriate balance between the relatively few industry standards, customer requirements (which is difficult if you have thousands of customers) and the ability to pass the test which should be evaluated before BLRT.

## **/ 4. BLRT Risk Assessment**

Because BLRT can be expensive and time-consuming, it is important to have performed a robust risk assessment before physical testing to ensure high confidence in BLRT success. But this can be challenging, if not impossible, for most semiconductor manufacturers because of the methods that are currently used to perform risk assessments. Specifically, most semiconductor manufacturers and their OSAT vendors use either overly complex three-dimensional (3D) finite element analysis (FEA) or overly simplistic reliability by similarity.

The use of 3D FEA within semiconductor manufacturers and OSATs has become increasingly important with the rise of additional complex semiconductor packaging including stacked die, system-in-package and through-silicon via. To successfully launch a 3D package, the industry needs to accurately capture electrical and thermal stresses and how they are influenced by die-package interaction. However, performing 3D FEA takes significant time and requires highly specialized experts. Semiconductor manufacturers typically only use 3D FEA on BLRT risk assessment for a very small subset of devices because 3D FEA cannot be used by the design team. These specialized experts use 3D FEA throughout the new product development process, most often in either high-profile programs or baseline programs in which multiple derivatives are spun off.

For all other programs, semiconductor manufacturers depend on reliability by similarity. If a new device is similar enough to a device that has passed BLRT, engineers may conclude that the new device will also pass BLRT. This approach carries risk as it relies on human judgment and questionable assumptions which could prove costly if the device fails BLRT.

Given the limitations of both techniques, several semiconductor manufacturers have transitioned to a third approach. This technique leverages physics-based, closed-form reliability equations, such as the Blattau Model, which either enables design teams to perform a BLRT risk assessment on their own or allows analyst teams to rapidly extrapolate existing 3D FEA results to a wider range of devices.

## **/ 5. BLRT Coupon Design**

One of the most unappreciated aspects of a successful BLRT — for both the device manufacturer and its customers — is the design of the test coupon.

The coupon thickness, coupon materials, coupon stackup, bond pad design and how the coupon is constrained can all play critical roles in passing BLRT while also being relevant to the most important customers. One classic example of this conundrum is the presence or absence of microvias under the BGA pad.

Once the solder ball pitch under a BGA drops to 0.5mm or below, almost all board-level designs require the use of microvias. While some designs can support a single layer of microvias, it is very common to have two or even three layers of microvias stacked on top of each other. These microvias can create an anchor to the solder ball, increasing the stiffness and greatly reducing the time to failure. However, most BLRT coupons have no microvias or a triple-stack. The result is devices passing JEDEC-style BLRT while failing Tier 1 or OEM qualification activities.

## **/ 6. Test Setup for BLRT is not Turnkey**

Finally, once all the test parameters have been selected and success has been confirmed, it is time to perform BLRT. However, testing is not as turnkey as one would expect. Despite designing a unique and specific test flow, other factors arise that require additional adjustments. Calibration approaches for attachment, monitoring techniques, monitoring frequency, temperature control across the chamber and failure definition are all critical for test relevance, test repeatability and acceptance by the broader industry. Furthermore, those factors are changing and developing at a rapid pace. This is where expansive industry BLRT experience and involvement are crucial to success.

Design teams already bear immense responsibilities during the design process which does not afford them the time or opportunity to continually refresh BLRT testing standards.

The key to implementing an efficient BLRT plan is operational intelligence that factors in the expectations of OEMs, suppliers and manufacturers across the industry to fully understand their needs.

This industry knowledge creates an expedited process for renewing testing standards at a pace that is consistent with speed of change and disruption. Keeping pace is key for implementing a fluid and ubiquitous testing plan that is repeatable.

## / Conclusion

Semiconductor manufacturers are in a bind: while there is accepted documentation to serve as a guide, there is a gap in the requisite qualifications between consumer products and automotive suppliers. For semiconductor manufacturers entering the automotive environment, the lack of universal qualifications standards often leads to inconsistent reliability expectations. The established standards are not wrong, rather, they do not address the complex and abundant automotive applications of today. Ansys-DfR Solutions has consistently found that the most efficient solution is to establish a robust and thorough BLRT testing plan that is uniquely designed for a specific manufacturer that is validated by a broad range of industry experiences.

BLRT should be tailored to apply to individual cases, rather than a general threshold. As the applications of semiconductor products diversify, the stresses they experience become increasingly vast. Because use environments are expanding rapidly, frequent and accurate testing with agreed upon expectations is essential for reliability success. However, goals are not always universally aligned throughout the supply chain. Considering OEMs, suppliers and manufacturers often have differing needs and priorities; an outside consultant specializing in BLRT can expedite time to market and cut costs given their understanding of the goals of each party involved.

Ansys Reliability Engineering Services performs over 550 reliability projects a year and has a unique capability to provide clear and robust advice on the right BLRT to semiconductor manufacturers and their customers across multiple markets.

If you are responsible for reliability testing, please contact us today to learn more about the turnkey implementation and execution of a BLRT plan in which manufacturers can have a high degree of confidence.

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