Solutions for PCB Electromagnetic Interference

Simulation Driven Product Development aids designers of printed circuit boards in meeting electromagnetic compatibility requirements.

By Steven G. Pytel, Jr., Signal Integrity Product Manager, ANSYS, Inc.

In today's world of highly complex printed circuit boards (PCBs), creating designs to meet electromagnetic compatibility (EMC) targets is a necessity. However, during the early design stage, development of a robust power delivery network (PDN) is often neglected. Minimizing board resonances using decoupling capacitors and the proper power and ground plane design will reduce radiated emissions that cause electromagnetic interference (EMI). Signal layout on the PCB is critical to correct operation of analog and digital designs and will help reduce radiated emissions while minimizing interference on other signal nets.

Designing to meet these three objectives with moderately to highly complex PCBs requires the use of simulation to minimize time to market and cost. SIwave software was developed specifically to provide solutions that help engineers meet the objectives of a robust PDN, sound signal integrity (SI) and EMI/EMC targets. Although SIwave is predominantly used for post-layout extraction, its drawing and clipping capabilities can be used to perform Simulation Driven Product Development for pre-layout simulation on partial designs. SIwave technology supports multiple PCB layout databases.

SIwave software's dynamic architecture allows it to fit seamlessly into most design processes while significantly reducing nonrecurring engineering costs. Designing a power distribution system (PDS) relies on several analysis types: resonant cavity analysis, network analysis and dc power loss analysis. The resonant cavity analysis provides an intuitive three-dimensional look at voltage differences between planes. For example, a user can quickly identify the location of resonances between planes to understand any voltage differences that are occurring between these planes. Depending on the resonance severity, the result can be detrimental to signaling causing increased emissions. Resonances cause a change in the ac board impedance. The resonances also cause reflections within signal lines, leading to an energy transformation that produces radiation.

Resonant Cavity Analysis

The voltage difference between the Vcc (positive voltage supply) — the large plane in Figure 2 — and ground is shown. In addition, another plane indicates the voltage difference between Vinput, (the smaller plane in the figure) and ground. The Vinput plane has a sharp resonance toward the upper right of the small plane, as circled. This could be problematic because it is occurring at the source of the switching field-effect transistor (FET) that converts the input power to dc. Identifying this resonance using cavity analysis provides the location where the network analysis should be performed so the SI designer can understand the ac impedance profile. A two-dimensional network analysis simulation was performed to view the impedance characteristics of the Vinput plane. A port was added to the surface of the board at the output of the FET. This connection was made between the Vinput and the ground pins of the device (Figure 3).

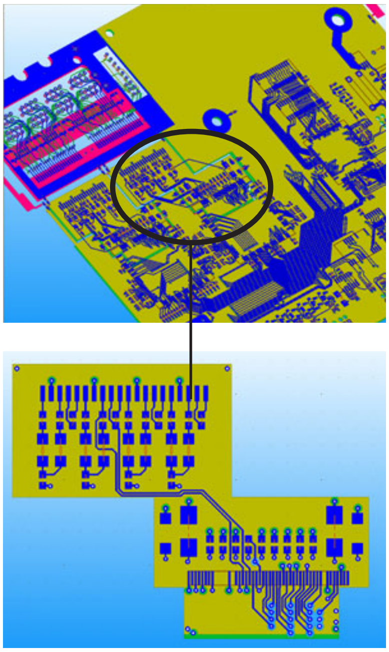


Figure 1: SIwave software displays a multilayer PCB imported from a layout design tool along with clipped microprocessor core power rail.

Network Analysis Solution

The network analysis solution option for passive devices uses a combination of computational electromagnetic solutions in conjunction with several modeling techniques to create accurate solutions. Passive devices can be modeled in three forms: simple (frequency independent), algorithmic (equation-based frequency dependent), and measured data (in the form of Touchstone® network parameters). The original design (Figure 5A) shows that the higher frequencies indicate a significant change in the impedance profile. The impedance

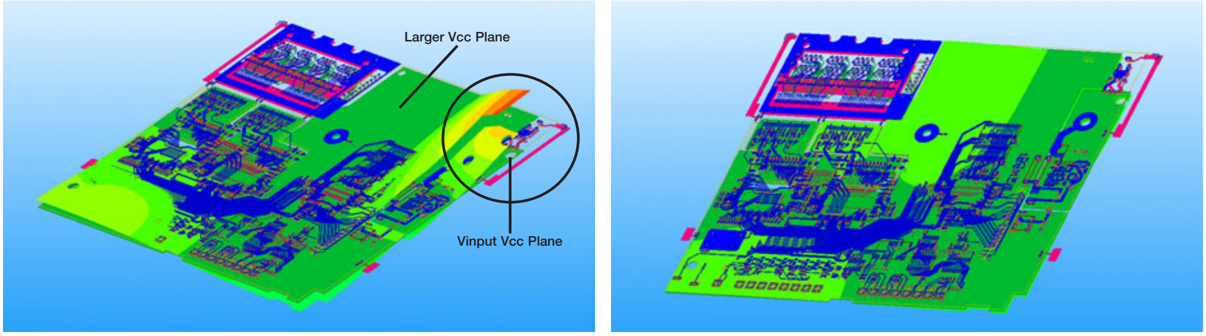


Figure 2: SIwave resonance analysis depicts the voltage differences between nets Vinput and ground (smaller plane) and nets Vcc and ground (larger plane). Resonant cavity analysis before (left) and after (right) addition of the decoupling capacitors

profile of the original solution goes from 1.5 ohms at 100 MHz to 105 ohms at 700 MHz. If there is a signal operating at or around 700 MHz that references this cavity, the signal will be severely degraded due to energy lost by the radiation of the fields. Adding a few decoupling capacitors between the Vinput and ground planes can significantly reduce the cavity resonance and improve signal quality while minimizing radiation. A good first-order approximation can be used to help decide what capacitor characteristics should be used to decouple the plane. Setting the inductive reactance equal to the capacitive reactance and solving for capacitance will help to obtain the capacitance needed. However, this requires the designer to make an approximation for the leakage and mounting inductance. This approximation is a good first-order solution, but a full-wave solution utilizing SIwave software will provide a much more accurate answer including a spatial dependence.

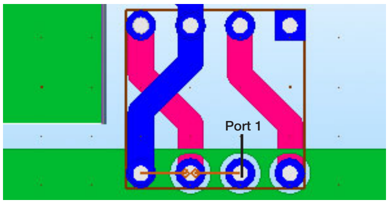


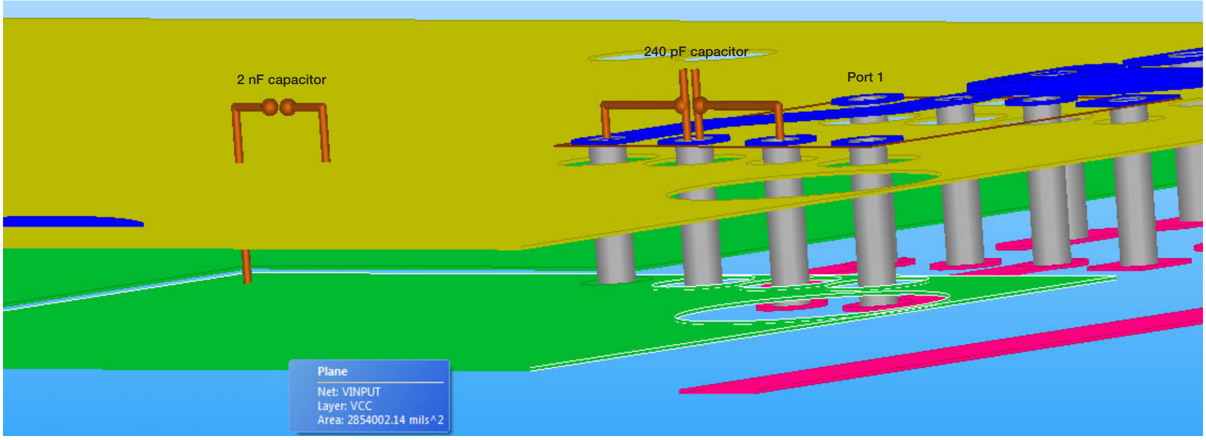
Figure 3: The addition of Port 1 for the network analysis solution between nets Vinput and ground

Using an approximation, a 240 pF capacitor with an assumed leakage and mounting inductance of 0.5 nH was placed across the Vinput and ground pins of the device (Figure 4). Figure 5B shows that, using the SIwave tool's full-wave network analysis, the large impedance variation has been greatly reduced at the higher frequencies. As expected, the resonance shifted slightly lower but with a much smaller magnitude (approximately 47 ohms). To further minimize this peak, a second decoupling capacitor of 2 nF with 0.5 nH leakage and mounting inductance was added to the upper left corner of the Vinput plane (Figure 5C).

This capacitor lowered the overall magnitudes of the resonance by a factor of five while shifting the resonance slightly lower and creating a smaller resonance about 8 MHz. To understand the decoupling impact on the entire Vinput plane, another resonance mode analysis was performed. The results from the resonant cavity analysis show the top half of the Vinput plane has been effectively decoupled using these techniques. The resonant mode analysis does not require any sources because it is focused on the natural cavities that occur within the board.

DC Power Loss

In addition to providing understanding of the power distribution system over frequency, SIwave software analyzes dc losses as well. Using a finite element method, the dc voltage drop, dc current density, and dc power loss across any plane, trace, or wirebond can be analyzed. This method considers nonideal return paths in its solution realizing that ground is relative within a PCB. The user selects the point(s) to which all solutions will be referenced (user defines earth/chassis ground). This allows the designer to analyze dc voltage, current, and power across voltage planes, ground planes, vias, and bondwires. In addition, the power loss can be exported to ANSYS Icepak software to study the effects of joule heating on the board. Flags can be set



Plane
Net: VINPUT
Layer: VCC
Area: 2854002.14 mils^2

Figure 4: Cutout view of the Vinput (green) and ground (gold) shows the physical location of Port 1, 240 pF capacitor and 2 nF capacitor.

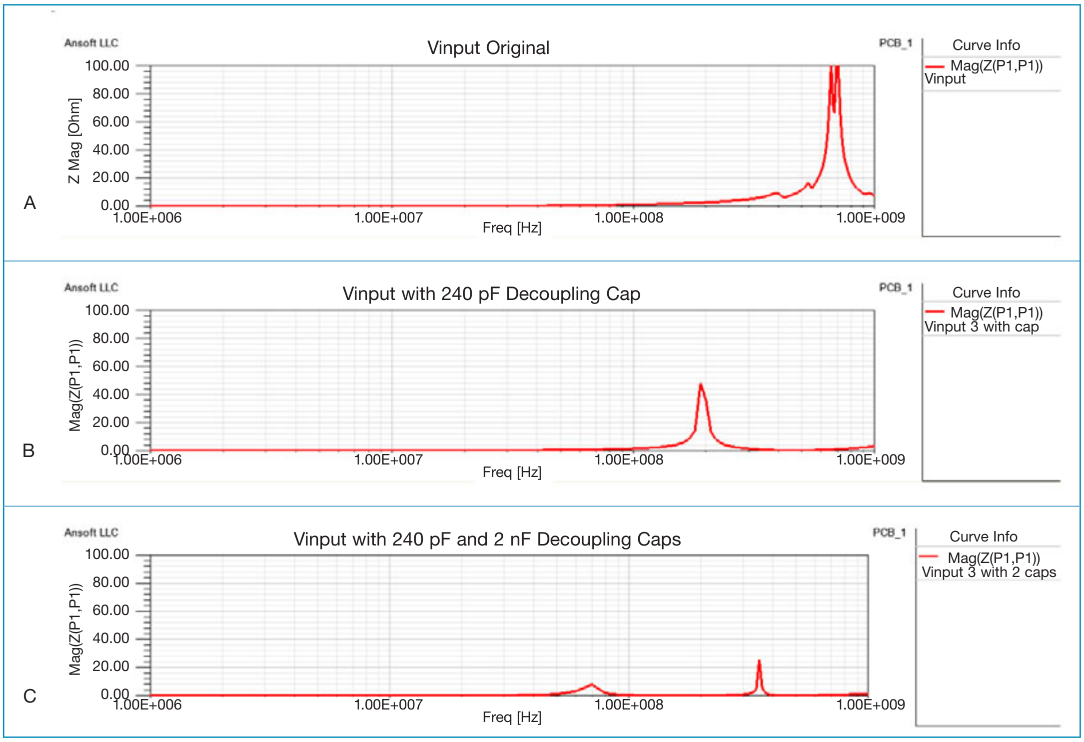


Figure 5: A) The original board design without any additional decoupling capacitors; B) analysis number two in which a 240 pF capacitor was added across the Vinput and ground pins of the FET device; C) analysis number three in which an additional 2 nF capacitor was added in the upper left corner of the Vinput plane

to show problematic areas that do not meet the specifications set forth by the designer. This can help to detect poor layout designs in which too few vias were used to connect power rails on different layers within the PCB, which may compromise reliability and lead to system failure.

With a properly designed power distribution system, EMI and signal quality issues are greatly reduced. A designer can change the focus from plane discontinuities to proper layout of signal traces that minimize coupling, reflections and insertion loss. A designer can adjust the frequency sweep, similar to the two-dimensional network analysis from power delivery, to study signal conditioning concerns over a broad frequency range. Many types of clocking architectures along with signal architectures can be analyzed, including, but not limited to, common clocking, source synchronous clocking, forwarded clocking, embedded clocking, including single-ended and differential (including planar and broadside coupling) transmission line topologies. Signal crosstalk (coupling), insertion, and return loss can be analyzed, while Touchstone and Full-Wave SPICE (FWS) files can be exported for usage in time domain circuit simulations. Near- and far-field simulations can be analyzed within SIwave software. These solutions accommodate frequency-independent and frequency-dependent voltage and current sources. The latter enables the designer to accurately quantify the power and frequency spectrum of switching devices. When used in combination with Ansoft Designer software, buffer models (analog and digital) can be used to automatically create the frequency domain power spectrum to be used with the near- and far-field analyses.

SIwave software's versatility allows it to seamlessly fit into almost any existing design flow for power distribution design, signal analysis and reduction of radiated fields. SIwave has the unique ability to bring three disciplines together (power integrity, SI and EMI/EMC design) in a single environment. This enables design engineers to make critical tradeoffs with a high degree of confidence prior to fabrication, minimizing time to market and design cost while ensuring robust designs that achieve first-pass system success. ■

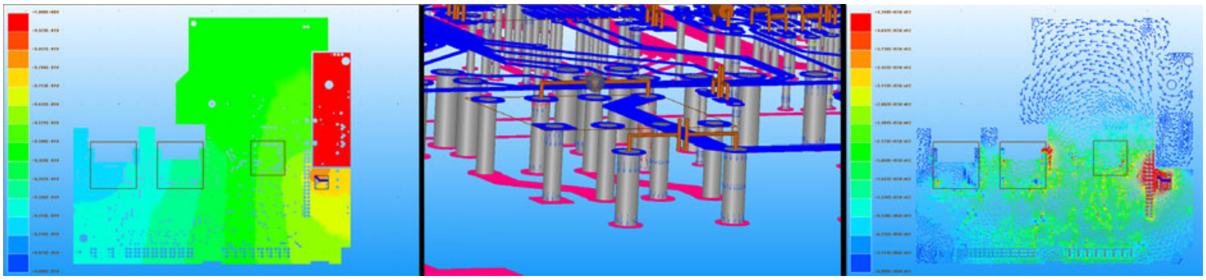


Figure 6: Dc analyses between the voltage regulator module (VRM) and the two microprocessors in the middle of the board show voltage drop across the plane (left), current flowing through the vias near the VRM (center), and current path from the VRM to the two microprocessors (right).